correcting (ECC) bit generated by the ECC code generator based on the at least one data bit in the memory cells.

REMARKS

Applicants appreciate Examiner Portka's willingness to conduct a telephone interview with the undersigned attorney on March 6, 2002. The following paragraphs contain a summary of the substance of that interview.

I. Pending Claims

Claims 104-125 are pending in this application. Applicants affirm the election of Claims 104-125 made by the undersigned attorney in a telephone conversation with Examiner Portka on October 29, 2001.

II. Information Disclosure Statement

Pending patent applications listed as documents A21-A26 accompanying the July 30, 2001 Information Disclosure Statement were lined out on the 1449 Form. It was suggested that the lined-out documents are more appropriately listed in the first section of the specification under the heading "Cross Reference to Related Applications." Applicants respectfully disagree.

Applicants wish the pending patent applications to be considered in the present application and made of record. MPEP 609(III)(A)(1) specifically states that pending patent applications should ***not*** be listed in the specification but rather should be listed on a 1449 form:

> The list of information complying with the identification requirements of 37 CFR 1.98(b) may not be incorporated into the specification of the application in which it is being supplied, but must be submitted in a separate paper [a 1449 Form]. A separate list is required so that it is easy to confirm that applicant intends to submit an information disclosure statement and because it provides a readily available checklist for the examiner to indicate which identified documents have been considered.

Additionally, 37 C.F.R. § 1.98, as recently amended, now makes clear that pending patent applications should be listed in a 1449 Form. Specifically, 37 C.F.R. § 1.98(a)(1)-(2) states that an information disclosure statement can cite a pending U.S. patent application, and 37 C.F.R. § 1.98(b)(3) describes how a pending U.S. patent application is to be listed in a 1449 Form. Documents A21-A26 were cited in accordance with these rules.

Applicants have enclosed, at Tab C, a 1449 form listing documents A21-A26 and request that the Examiner initial this form and return a copy of the initialed form to the undersigned attorney along with the next communication.

III. Amendments to the Specification

It was requested that Applicants update the application numbers and status of co-pending applications listed in the specification. In this Amendment, Applicants have amended the paragraphs on page 1, lines 3-4; page 3, lines 14-28; page 8, lines 23-30; page 9, lines 13-26; and page 18, lines 14-23 to make the requested changes.

IV. Claim Rejections under 35 U.S.C. §112, First Paragraph

Claims 107, 112, 116, and 119 were rejected under 35 U.S.C. §112, first paragraph, as containing subject matter that was not described in the specification in such a way as to enable one skilled in the art to make and use the invention. These claims each recite that the memory is selected from a group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and a organic-electronics-based memory device. In the Office Action, it was asserted that the application did not disclose how these devices are implemented as write-once and/or three-dimensional devices. Applicants respectfully disagree.

Page 3, lines 21-25 of Applicants' specification incorporates several patent documents by reference that describe three-dimensional write-once memory devices. One of those documents, U.S. Patent No. 6,034,882 to Johnson et al., teaches how to implement a semiconductor-transistor-technology-based memory device as a write-once three-dimensional device. See, for example, columns 7-10, which describe a semiconductor-transistor-technology-based write-once memory cell, and columns 19-21, which teach three-dimensional organization of such memory cells. Since Johnson et al. is incorporated by reference in the present application, the enabling disclosure provided in Johnson et al. is part of the present application. See MPEP 608.01(p) (material that provides an enabling disclosure of the claimed invention can be incorporated by reference into an application by reference to a U.S. patent). In regard to magnetic- and organic-electronics-based memory devices, Applicants submit that one reasonably skilled in the art could implement these devices as write-once and/or three-dimensional devices given the disclosure discussed above coupled with information known in the art without undue experimentation. See MPEP 2164.01.

In summary, because the application provides an enabling disclosure of Claims 107, 112, 116, and 119, the 35 U.S.C. §112, first paragraph, rejections of those claims should be removed.

V. 35 U.S.C. §102(b) Rejections of Independent Claims 104 and 109

Independent Claims 104 and 109 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,796,694 to Shirane and also by U.S. Patent No. 5,835,509 to Sako et al. In both Shirane and Sako et al., the write-once memory device is an optical disc. Applicants have amended Claims 104 and 109 to recite that the write-once memory device is an electronic memory device. During the telephone interview, it was agreed that this amendment would overcome the §102(b) rejections of Claim 104 and 109.

The Examiner and the undersigned attorney also explored the reasons why one skilled in the art would not have modified Shirane and Sako et al. to yield the claimed invention. For example, with respect to Shirane, one skilled in the art would have had to (1) replace the optical disc 15 with an electronic memory device and (2) remove the system controller 11, which implements the ECC functionality, from the disc drive 17 and integrate it in the electronic memory device. However, one skilled in the art would not have been motivated to take an electronic component intended to be a permanent part of the disc drive 17 and place it in a memory device that can be removed from the disc drive 17. This would result in the disc drive 17 being unable to provide ECC protection if a memory device without ECC circuitry were used in the disc drive 17. In this regard, the Examiner suggested that Applicants amend Claims 104 and 109 to clarify that the recited electronic memory device is modular and releasably connected to a data storage system. Applicants have amended Claims 104 and 109 in accordance with the Examiner's suggestion. The Examiner also suggested that Applicants clarify that the ECC code circuitry and the memory unit are in the same device. Further to this suggestion, Applicants have amended Claims 104 and 109 to recite that the ECC code circuitry and the memory unit are carried by the same support element and that the memory device has a modular housing that protects the ECC code circuitry and the memory unit.

VI. 35 U.S.C. §102(b) Rejections of Independent Claims 114, 117, and 120

Independent Claims 114, 117, and 120 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,432,729 to Carson et al. During the telephone interview, Applicants explained the differences between the "three-dimensional" multichip structure disclosed in Carson et al. and the three-dimensional memory device recited in Claims 114, 117, and 120. In summary, the three-dimensional multichip structure in Carson et al. is nothing more

than several individual memory chips stacked and secured together. Although the shape of the overall structure is three-dimensional, the memory arrays within it are not. Each of the memory chips in the structure has a two-dimensional memory array, and stacking chips together does not transform two-dimensional memory arrays into a three-dimensional memory array. In contrast, the memory cells in Applicants' three-dimensional memory device are stacked vertically above one another in a single chip. To emphasize this difference, Applicants have amended Claims 114, 117, and 120 to recite that the memory device comprises a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip. During the telephone interview, the Examiner agreed that this amendment would overcome the 35 U.S.C. §102(b) rejections based on Carson et al.

As a further ground of patentability, Applicants have amended Claims 114, 117, and 120 to recite elements that were added in this Amendment to independent Claims 104 and 109. Specifically, the memory device is now recited to be a modular, electronic memory device adapted to be releasably coupled to a data storage system. Additionally, Applicants have clarified that the modular, electronic memory device comprises a housing that contains ECC code circuitry (Claims 114 and 117) and a memory unit (Claims 114, 117, and 120). These amendments provide additional elements that are not taught or suggested by the cited references.

VII. Conclusion

In view of the foregoing amendments and remarks, Applicants submit that the present application is in condition for allowance. Reconsideration is respectfully requested. If the Examiner has any questions concerning this Amendment, he is asked to contact the undersigned attorney at (312) 321-4719.

Dated: March 27, 2002

Respectfully submitted,

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APPENDIX B

104. (Amended) A modular, electronic write-once memory device adapted to be releasably connected to a data storage system, the modular, electronic write-once memory device comprising:

a support element;

error checking and correcting (ECC) code circuitry carried by the support element; [and]

a memory unit carried by the support element and comprising a plurality of write-once memory cells, wherein at least one data bit and at least one ECC bit generated by the ECC code circuitry based on the at least one data bit are stored in the plurality of write-once memory cells; and

a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit.

106. (Amended) The invention of Claim [105] 104, wherein the [electronic memory device comprises a three-dimensional electronic memory device] plurality of write-once memory cells are arranged in a plurality of layers stacked vertically above one another in a single chip.

107. (Amended) The invention of Claim [105] 104, wherein the electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and an organic-electronics-based memory device.

109. (Amended) A method for storing data and error checking and correcting (ECC) code bits in a modular, electronic write-once memory device, the method comprising:

providing a modular, electronic write-once memory device adapted to be releasably connected to a data storage system, the modular, electronic write-once memory device comprising a support element, error checking and correcting (ECC) code circuitry carried by the support element, and a memory unit carried by the support element and comprising a plurality of write-once memory cells;

with [a] the modular, electronic write-once memory device, receiving at least one data bit to be stored in the write-once memory [device] cells;

with the ECC code circuitry [integrated with the write-once memory device], generating at least one ECC bit based on the at least one data bit; and

storing the at least one data bit and the at least one ECC bit in the write-once memory [device] cells.

111. (Amended) The invention of Claim [110] 109, wherein the [electronic memory device comprises a three-dimensional electronic memory device] plurality of write-once memory cells are arranged in a plurality of layers stacked vertically above one another in a single chip.

112. (Amended) The invention of Claim [110] 109, wherein the electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and an organic-electronics-based memory device.

114. (Amended) A modular three-dimensional electronic memory device adapted to be releasably connected to a data storage system, the modular three-dimensional electronic memory device comprising:

a support element;

error checking and correcting (ECC) code circuitry carried by the support element; [and]

a memory unit carried by the support element and comprising a plurality of memory cells arranged [in the three-dimensional electronic memory device] in a plurality of layers stacked vertically above one another in a single chip, wherein at least one data bit and at least one ECC bit generated by the ECC code circuitry based on the at least one data bit are stored in the plurality of memory cells [arranged in the three-dimensional electronic memory device]; and

a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit.

115. (Amended) The invention of Claim 114, wherein the memory cells comprise [three-dimensional electronic memory device comprises a] write-once memory [device] cells.

116. (Amended) The invention of Claim 114, wherein the [three-dimensional] modular, electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and an organic-electronics-based memory device.

117. (Amended) A method for storing data and error checking and correcting (ECC) code bits in a [three-dimensional] modular, electronic memory device, the method comprising:

providing a modular, electronic memory device adapted to be releasably connected to a data storage system, the modular, electronic memory device comprising a support element, error checking and correcting (ECC) code circuitry carried by the support element, a memory unit carried by the support element and comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip, and a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit;

with [a three-dimensional] the modular, electronic memory device, receiving at least one data bit to be stored in the [three-dimensional electronic] memory [device] cells;

with the ECC code circuitry [integrated with the three-dimensional electronic memory device], generating at least one ECC bit based on the at least one data bit; and

storing the at least one data bit and the at least one ECC bit in the [three-dimensional electronic memory device] memory cells.

118. (Amended) The invention of Claim 117, wherein the memory cells comprise [three-dimensional electronic memory device comprises a] write-once memory [device] cells.

119. (Amended) The invention of Claim 117, wherein the [three-dimensional] modular, electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and a organic-electronics-based memory device.

120. (Amended) A system for storing an error checking and correcting (ECC) bit in a three-dimensional memory array of memory cells in a memory device, the system comprising:

a data storage system; and

a modular, electronic memory device adapted to be releasably coupled to the data storage system, the modular, electronic memory device comprising:

[a three-dimensional memory array] a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip; and

a modular housing protecting the three-dimensional memory array;

wherein the [a] data storage system [coupled with the memory device and comprising] comprises an error checking and correcting (ECC) code generator [, wherein the data storage system] and is operative to store at least one data bit and at least one error checking and correcting (ECC) bit generated by the ECC code generator based on the at least one data bit in the [three-dimensional] memory [array in the memory device] cells.